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PATENT & TRADEMARK OFFICE

FIG 10

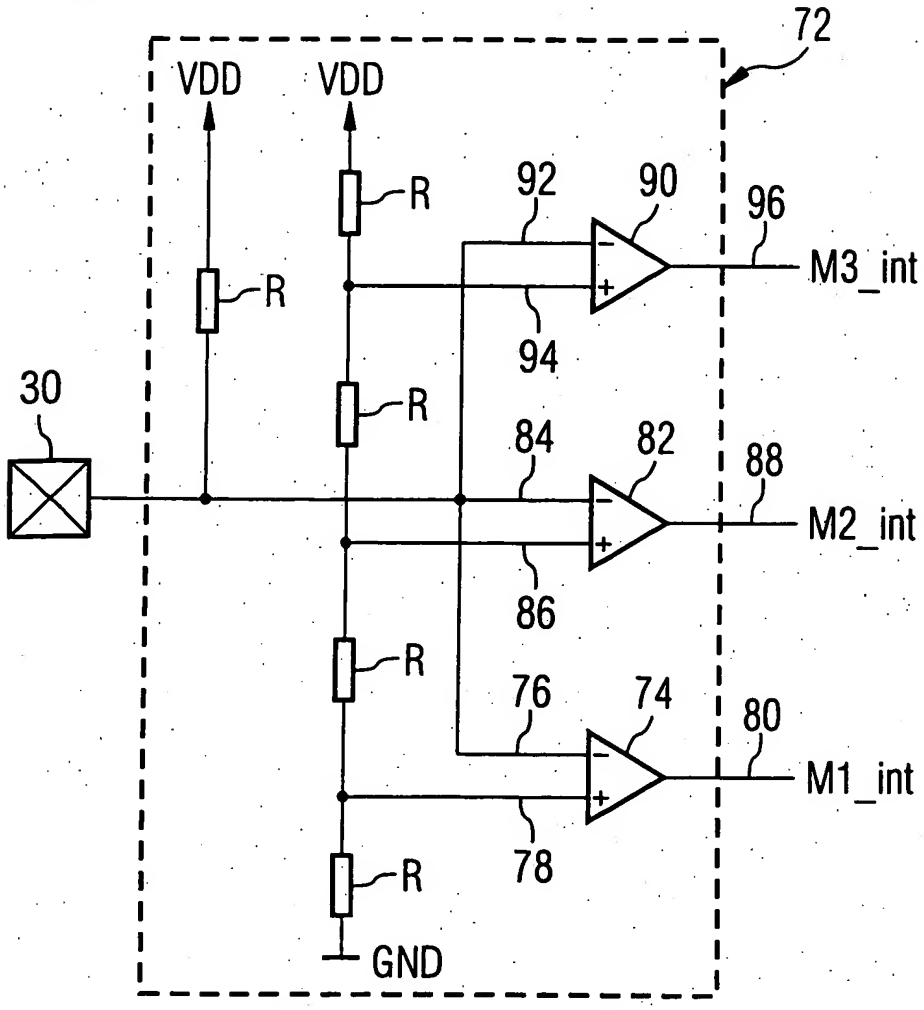

FIG 11

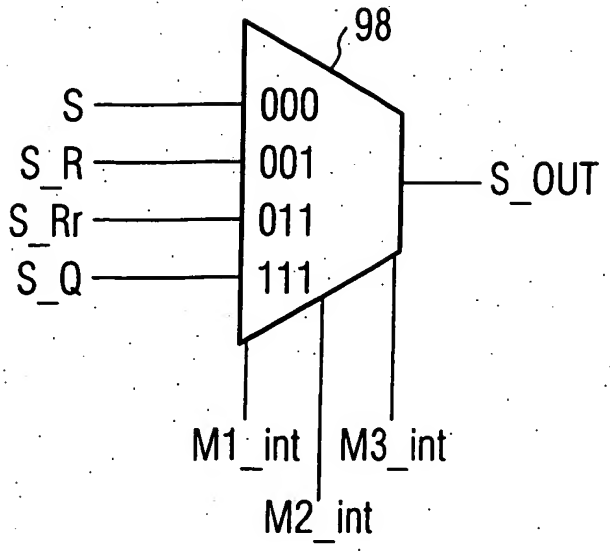

FIG 12

M1_int	M2_int	M3_int	S_OUT
0	0	0	S
0	0	1	S_R
0	1	1	S_Rr
1	1	1	S_Q